# COMP3500: TLB and Memory Access

**🟊: >85%, 🟊🟊: 70-85%, 🟊🟊🟊: 55-70%, 🟊🟊🟊🟊: 40-55%, 🟊🟊🟊🟊🟊: < 40%**

**🟊🟊🟊🟊🟊 Exercise 1 (Plickers):** We assume that page size is 4KB (i.e., 212), each page table entry is 4 bytes. How large is the page table for a 32-bit logical address space?

A. 1 MB B. 2 MB C. 4 MB D. 8 MB

**🟊🟊🟊 Exercise 2 (Plickers):** We assume that page size is 1KB (i.e., 210), each page table entry is 8 bytes. How large is the page table for a 64-bit logical address space?

A. 254 Bytes B. 255 Bytes C. 256 Bytes D. 257 Bytes

**🟊🟊 Exercise 3 (Plickers):** Why TLBs are typically small (64 to 1,024 entries)?

A. Program is small

B. Cost is high

C. Address space is small

D. Performance is high

**🟊🟊🟊🟊🟊 Exercise 4 (Plickers):** Why some TLBs storeaddress-space identifiers (**ASIDs**)in each TLB entry – uniquely identifies each process?

1. High performance
2. Low cost
3. Security projection
4. High scalability

**🟊 Exercise 5 (Plickers):** What happens on a TLB miss?

A. There will never be a TLB miss

B. Replace an existing TLB entry

C. Schedule the entries in TLB

D. There will be a page table miss

**🟊 Exercise 6:** Consider a single-level paging scheme with no data cache. The TLB has 32 entries. The TLB access time is 10 ns; memory access time is 200ns.

* 1. **(Plickers)** How long does it take to access data in memory if there is a TLB hit?

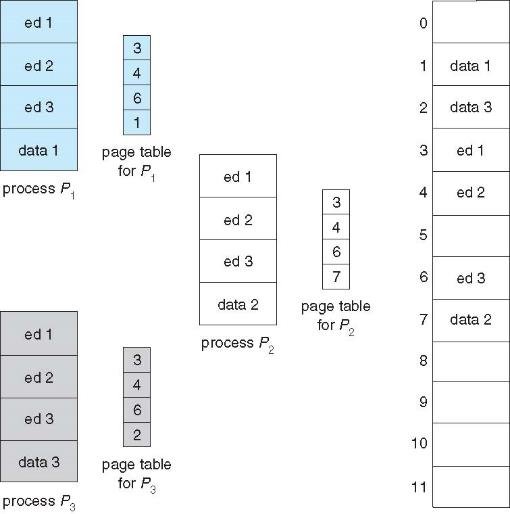
1. 210ns B. 200ns C. 190ns D. 220ns
   1. **(Plickers)** How long does it take to access data in memory if there is a TLB miss?
2. 200ns B. 210ns C. 400ns D. 410ns

6.3 What is the effective memory-access time if we have a TLB hit ratio of 80%? Effective memory-access time indicates the average amount of time a memory access takes. (see Silberschatz, et al)

6.4 What is the minimal hit ratio that will guarantee the effective access time of at most 220ns?

**Exercise 7:** How can we also indicate a page is execute-only or not?

**Exercise 8:** What do you observe from the following three page tables?



**Exercise 9:** What happens if two page numbers are hashed to the same location?

**Exercise 10:** How to improve performance of the inverted page table?

